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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/590,462 | 06/09/2000 | Marco Racanelli | 02SPE133P | 1783 |

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| EXAMINER | |
|---|---|
| DIAZ, JOSE R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/590,462 | RACANELLI ET AL. | |
| | Examiner | Art Unit | |
| | José R. Díaz | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-9,17,19,20,22,26,27,29 and 31-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,17,19,20,22,26,27,29 and 31-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 15, 2005 has been entered.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 17, 20 and 27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the instance case, the limitation of forming a contact layer of a first conductivity type is not supported by applicant's disclosure. Please note that the disclosure only provides support for a contact having a second conductivity type (see page 7, lines 27-31 of applicant's specification). Please note that

in the rejections below, claim 17, 20 and 27 will be rejected based on the supported description.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-2, 6, 9, 19, 22, 26, 29, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shannon (US Pat. No. 3,761,319) in view of Pfander et al. (US Pat. No. 3,581,164), and further in view of Minotani (JP 56-26477).

Regarding claims 1, 6, 9, 26, 33 and 35, Shannon teaches a method of forming a varactor device on a semiconductor substrate, comprising the steps of:

forming a buried layer (86) in said semiconductor substrate (81), said semiconductor substrate having a first conductivity type (P-type) and said buried laver having a second conductivity type (N-type) (see fig. 9);

providing an epitaxial layer (83) situated in said semiconductor substrate, said epitaxial layer having said first conductivity type (P-type), wherein said epitaxial layer is situated over said buried layer (86) (see fig. 9);

providing an isolation structure (85) on said semiconductor substrate (see fig. 9), said isolation structure defining an implant region (91, 92), said implant region being situated over said epitaxial layer (83) (see fig. 10);

selecting a first peak dopant concentration (consider the selected dose $1 \times 10^{14}$ $cm^{-2}$, which inherently result in a region of a specific dopant concentration) and a first implant energy (100 kev) (col. 14, lines 56-59);

forming a first implant in said epitaxial layer (100) using said first implant energy (100 kev) (col. 14, lines 56-59), said first implant having said first peak dopant concentration (P) and said first conductivity type (P-type), wherein said first implant extends into said epitaxial layer (83) a first distance, and wherein said first implant is situated over said buried laver (86) (see fig. 11).

In addition, Shannon teaches that it is very well known in the art to form doped region by ion implantation and annealing (see col. 1, lines 49-53 and col. 2, lines 5-13).

However, Shannon fails to teach the steps of: optimizing least one of capacitance, leakage current, and tuning range of the varactor device; and forming a second implant in said epitaxial layer using a second implant energy, said second

implant having a second peak dopant concentration and said first conductivity type, wherein said second implant extends into said epitaxial layer a second distance, wherein said second distance is greater than said first distance, wherein said second implant is situated over said buried layer, and wherein said second implant has a depth that is more than twice a depth of said first implant.

Pfander et al. teaches that it is well known in the art to form a second P-type region (8) beneath the emitter region (5) (see fig. 1); wherein the region (8) has a depth that is more than twice a depth of a first P-type region (4) (consider the depth of regions 4 and 8, in fig. 1); and to select a peak dopant concentration such that at least one of capacitance, leakage current, and tuning range of the varactor device is optimized [please consider the dopant concentration shown in curves A corresponding to region 8 and curve B corresponding to region 4 in fig. 2, which form a varactor having an optimized junction capacitance (col. 3, lines 25-48 and abstract)]. The motivation for doing so, as is taught by Pfander et al., is to double the capacitance without increasing the semiconductor surface area (col. 4, lines 53-56).

Shannon and Pfander et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include the steps of: selecting a first peak dopant concentration and a first implant energy such that at least one of capacitance, leakage current, and tuning range of the varactor device is optimized; forming a second implant in said epitaxial layer using a second implant energy, said second implant having a second peak dopant concentration and said first conductivity

type, wherein said second implant extends into said epitaxial layer a second distance, wherein said second distance is greater than said first distance, wherein said second implant is situated over said buried layer, and wherein said second implant has a depth that is more than twice a depth of said first implant. The motivation for doing so, as is taught by Pfander et al., is to double the capacitance without increasing the semiconductor surface area (col. 4, lines 53-56). Therefore, it would have been obvious to combine Pfander et al. with Shannon to obtain the invention of claims 1-2, 6, 9, 19, 22, 26, 29, 33 and 35.

Regarding claims 2 and 29, Pfander et al. teaches the formation of a second doped region (8) in the first doped region (4) (see fig. 1); and Shannon teaches the steps of implanting and annealing to form the desired doped region (see col. 1, lines 49-53 and col. 2, lines 5-13). With regards to the claimed limitation of minimizing the base resistance of the varactor, please note that the formation of the second doped region (8) in a base region (4) inherently reduces the resistance in the base region.

Regarding claims 19 and 22, Pfander et al. teaches isolation structure comprising CMOS well (7) (see fig. 1).

7. Claims 4-5, 7-8, 31-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shannon (US Pat. No. 3,761,319) in view of Pfander et al. (US Pat. No. 3,581,164), and further in view of IBM Corporation (NN79013241), "Determination of Doping Profiles by Means of SIMS", IBM Technical Disclosure Bulleting, 1979, Vol. 21, Issue Number 8, p. 3241-3242.

Regarding claims 4-5, 7-8, 31-32 and 34, a further difference between the prior art and the claimed invention is using a secondary ion mass spectroscopy (SIMS) to determine the dopant concentration profile. However, IBM Corporation (NN79013241) teaches that SIMS is a well-known technique use for determining doping concentrations and their respective depth (see last sentence of the "DISCLOSURE TEXT").

Shannon, Pfander et al. and IBM Corporation (NN79013241) are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to determine the dopant concentration profile of the first and second implants by using secondary ion mass spectroscopy (SIMS). The motivation for further doing so, as is taught by IBM Corporation (NN79013241), is determining the doping profile of the wafer (see lines 1-3 of the "DISCLOSURE TEXT"). Therefore, it would have been obvious to further combine IBM Corporation (NN79013241) with Shannon and Pfander et al. to obtain the invention of claims 4-5, 7-8, 31-32 and 34.

8. As far as understood, claims 17, 20, 27 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shannon (US Pat. No. 3,761,319) in view of Pfander et al. (US Pat. No. 3,581,164), and further in view of Kubo (US 2002/0014650 A1).

Regarding claims 17, 20, 27 and 36, a further difference between the prior art and the claimed invention is the step of forming a contact layer of a second conductivity type. However, Kubo teaches that it is well known in the art to form an emitter region by forming a polysilicon layer (20) doped of a second conductivity type (N-type) (see fig.

4B), and then heating the polyslicon layer to diffuse the N-type dopant in the substrate to form the emitter region (14) (see fig. 4C).

Shannon, Pfander et al. and Kubo are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the emitter region by forming a polysilicon layer doped with a second conductivity type, and heating the polyslicon layer to diffuse the dopant in the substrate to form the emitter region. The motivation for further doing so, as is taught by Kubo, is reducing the manufacturing steps process (see paragraph [0043]). Therefore, it would have been obvious to further combine Kubo with Shannon and Pfander et al. to obtain the invention of claims 4-5, 7-8, 31-32 and 34.

### *Response to Arguments*

9. Applicant's arguments with respect to claims 1-2,4-9,17,19-20,22,26-27,29, and 31-36 have been considered but are moot in view of the new grounds of rejection.

### *Conclusion*

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Minotani (JP 56-26477) teaches a varactor having a plurality of doped regions (15, 17, 19) (see fig. 6); Enosawa et al. (JP 56-042381 A) discloses a varactor having a plurality of diffused regions (9 and 10) (see figs. 2 and 3); and Igarashi et al. (JP 04-343479) discloses a varactor in figures 1 and 2.

***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/2/05

José R. Díaz
Examiner
Art Unit 2815